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STRUCTURE AND METHOD OF MAKING STRAINED SEMICONDUCTOR CMOS TRANSISTORS HAVING LATTICE-MISMATCHED SOURCE AND DRAIN REGIONS

Abstract

A p-type field effect transistor (PFET) and an n-type field effect transistor (NFET) of an integrated circuit are provided. A first strain is applied to the channel region of the PFET but not the NFET via a lattice-mismatched semiconductor layer such as silicon germanium disposed in source and drain regions of only the PFET and not of the NFET. A process of making the PFET and NFET is provided. Trenches are etched in the areas to become the source and drain regions of the PFET and a lattice-mismatched silicon germanium layer is grown epitaxially therein to apply a strain to the channel region of the PFET adjacent thereto. A layer of silicon can be grown over the silicon germanium layer and a salicide formed from the layer of silicon to provide low-resistance source and drain regions.